REMARKS

Applicant has canceled dependent claims 8, 19 and 20 and added independent claim 21 and dependent claims 22-24. It is believed that applicant should be charged for one extra claim since four was added and three taken away and applicant is allowed a third independent claim without an extra charge. In any case please charge any fees for additional claims which may be required to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

There are several ways in which heat transfer to the substrate from self-heating (Joule heating) in metal lines can be improved to lower temperature increases and thereby provide improved reliability. One way is to make an intimate thermal contact with the substrate as is believed in the two references. In the Kazami reference, the intimate thermal contact is intended to be made while not having any negative electrical impact on the electrical functionality. That is, even though it comes into contact with the substrate, it is supposed to act as a completely open circuit electrically. In the Jensen reference, a similar contact is made, in the context of a packaging scheme. The Jensen reference totally avoids any discussion about the electrical contact between the circuit body 10 and the package body 12. Presumably it just accepts that there is an electrical connection. The metallic trace 20 makes contact with the heat sink 12.

There are some potentially negative consequences in the Kazami reference for the scheme described. There are two main embodiments in the Kazami reference. In the first, the heat pipe described touches the substrate without any additional doping added to the substrate where it touches. In the second embodiment, additional doping of opposite

conductivity type is added to the substrate surface region, presumably to make the touching region look more like an infinite resistance by creating a p-n junction. Both of these schemes have potential negative consequences. A metal in contact with a semiconductor forms a Schottky barrier diode and such a diode always has a voltage polarity which passes small amounts of current, and an opposite voltage polarity passes large amounts of current. The real weakness of the Kazanmi reference is that the Schottky barrier diode can allow carrier injection from undesired pulses, such as ESD pulses, or even possibly switching transients on the electrically active portion of the lead to which the heat pipe is attached. Carrier injection is the cause of latchup in CMOS circuits. Any touching of the substrate by the heat pipe could lead to such consequences.

In applicant's teaching there is never any attempt to touch the heat sinking substrate. There is always some portion of the dielectric material separating the inactive conductor or fin from the heat sinking substrate and, of course, from unrelated metal lines. Applicant's teach and claim the non-current carrying extensions of metal lines are designed to improve heat flow to the substrate. Heat flow is improved by the non-current carrying extensions is several ways. For an isolated case (in the absence of neighboring metal lines), the closer the fins or electrically inactive conductors are to the substrate (while still maintaining dielectric isolation) and the larger the spatial area above the substrate, the more efficient the heat transfer to the substrate. In a non-isolated case (in the presence of neighboring metal lines), in which the heat generating line and fin in question is embedded amongst other electrically unrelated metal lines, the heat transfer can also occur to these other metal lines if they themselves are not also being heated by Joule heating. Any circuit design layout has a pre-defined heat generating aspect due to

Joule heating in the lines and heat dissipating aspect due to heat flow from the lines to the substrate. The addition of the electrically inactive metal lines or fins to the active lines which has excessive heating improves the heat dissipating qualities of the overall structure. The electrically inactive metal lines or fins provide an enhanced heat dissipating structure. Due to interactions with neighboring lines of any kind, heat will be more efficiently removed, as long as the neighboring lines do not themselves have excessive heat generation through Joule heating.

Applicant's claim 1 calls for "providing an enhanced heat dissipating structure comprising a continuous electrically inactive conductor extending in one or more heat dissipating layers of a dielectric body dielectrically spaced from and along a heat dissipating substrate and connecting said electrically inactive conductor to said electrically active interconnect line as an extension of said electrically active interconnect line to dissipate heat from said electrically active interconnect line through said enhanced heat dissipating layers of dielectric body. "

Clearly this is not taught in the cited references. The thermal transfer is though the metallic trace 20 in Jensen and through the contact 5A in Fig. 1 of Kazami and the PN junction of Kazami in the other figures. The heat is not dissipated through an enhanced heat dissipating structure comprising a continuous electrically inactive conductor extending in one or more heat dissipating layers of a dielectric body dielectrically spaced from and along a heat dissipating substrate. The electrical isolation is provided by the dielectric material. This is a different type of aided heat transfer not anticipated by these references.

In Jensen a solder ball or fillet 14 connects a contact pad 16 of the integrated circuit chip 10to the metallic trace 20 to the heat sink 12 and therefore the thermal transfer is through the solder fillet 14 and the metallic trace to the heat sink 12. The raised feature 22 extends from the lower layer 26 toward the underlying heat sink 12.

In the Kazami reference the structure 5 consists of a contact 5A, vias 5C, 5E, 5G, and 5I, and small portions of metal segments (5B, 5D, 5F, and 5H). The latter are necessary as part of the no-additional-step-added-to-the-process-flow to complete a complete thermal pipe from the bottom of lead 2, through the top of via 5I, and conducting heat downward through the bottom of contact 5A into the substrate where the contact 5A and the substrate 9 touch. The examiner refers to 5B, 5D, 5F, and 5H as "horizontally arranged heat dissipating layers" and 5A, 5C ,5E, 5G, and 5I as "electrically inactive conductors" but that language is not used. The truth is that the entire heat pipe structure 5 and each of its elements are heat dissipating layers (because they are metal) and they are all electrically inactive conductors, but only to the extent that there is no carrier injection into the substrate from any intentional or unintentional (such as pulses that cause ESD damage) transients. Kazami repeatedly emphasizes both in the specification and claims that the invention involves touching of the heat pipe to the substrate. That is the sole function achieved by the Kazami reference. In the first claim of this reference, it mentions "electrically non-connected heat sinking wiring extending ...to a silicon substrate..." In claim 2 of this reference, it mentions the use of a PN junction to supposedly improve the electrical characteristics caused by such touching. In claim 4 of this reference, it specifically says, "wherein the heat sinking wiring is in contact with the

silicon substrate while avoiding the contact of the heat sinking wiring with the oxide layer provided on the surface of the silicon substrate."

Applicant's invention does exactly what Kazami teaches to avoid. Applicant's invention teaches to remove contact 5A and to make the metal segments 5B, 5D, 5F and 5G extend horizontally to the right as far over to the structure 6A as design rules would allow to increase their surface area. These extended segments would then be the fins of applicant's invention. They would never make direct physical contact to the substrate, so there is never any issue about adverse carrier injection into the substrate. All heat loss is ultimately through some dielectric layers separating the fin from the substrate, or through some dielectric layer(s) to neighboring lines such as to the structure 6A, which can then conduct directly to the substrate.

Clearly, applicant's claimed invention is not obvious in view of these references. In view of the above applicant's claim 1 is deemed allowable over the references.

Claims 2-7 and 9-12 dependent on claim 1 are deemed allowable for at least the same reasons as claim 1. Claim 2 further calls for "said electrically inactive conductor is on one or more enhanced heat dissipating layers of said dielectric body that are closer to a heat dissipating substrate than said electrically active interconnect line." This is not taught in the references.

Claim 3 calls for "said electrically inactive conductor is connected to said electrically active interconnect line using one or more vias through one or more layers of said dielectric body."

Claim 4 calls for "wherein said electrically inactive conductor is connected to said electrically active interconnect line using at least two vias and a conducting pad through two or more layers of said dielectric body."

Claim 5 further calls for "said dielectric body includes dummy metal structures and said electrically inactive conductor is spaced from and aligned with one or more of said dummy metal structures to aid in dissipating heat from said electrically inactive conductor.

The examiner makes some comments about dummy metal. The examiner refers to structures 5B, 5D, 5F, and 5H as dummy metal. This is not dummy metal. Dummy metal is additional metal patterned on a metal level that is not physically connected to any metal line and patterned to achieve an electrical function in a circuit design. Dummy metal is placed in regions where active metal lines are needed in order to improve the metal coverage (fractional portion of area covered by metal) in the vicinity of patterned electrically active leads in order to improve process uniformity, line-width control, and pattern shape, particularly during the process called Chemical-Mechanical Processing (CMP) in copper based technologies. Kazami makes no reference to dummy metal at all.

Claim 6 further calls for "said dummy metal structures is in said dielectric body between said electrically inactive conductor and said heat dissipating substrate."

Claim 7 further calls for "The method of claim 2 including the step of coupling said heat dissipating substrate to a heat sink."

Claim 9 calls for "said electrically inactive conductor is in a straight line."

Claim 10 further calls for "said electrically inactive conductor is not in a straight line."

Claim 11 further calls for "said electrically inactive conductor is in the shape of an H with two parallel conductors and a cross connector connected to the electrically active connector."

Claim 12 further calls for " said electrically inactive conductor is in a heat dissipating dielectric layer of said dielectric body adjacent to said electrically active conductor and wherein said electrically inactive conductor and a via connection to the electrically inactive conductor is formed by a damascene process."

Claim 13 calls for "An integrated circuit, comprising:
an electrically active interconnect line within a dielectric body having a top and bottom surface, the bottom surface of the dielectric body being coupled to the top surface of a heat dissipating substrate underlying the dielectric body; and
an electrically inactive continuous conductor within said dielectric body at one or more layers of said body closer to the heat dissipating substrate than said active interconnect line with dielectric material separating the inactive conductor from said heat dissipating substrate; said electrically inactive conductor coupled to said electrically active interconnect line as an extension of electrically active interconnect line to dissipate heat therefrom."

For the reasons discussed above in connection with claim 1, the references do not teach or suggest "an electrically inactive continuous conductor within said dielectric body at one or more layers of said body closer to the heat dissipating substrate than said active interconnect line with dielectric material separating the inactive conductor from said heat dissipating substrate."

Claims 14-18 dependent on claim 13 are deemed allowable for at least the same reasons as claim 13.Claims 14 further call for vias providing the connecting between the ative and inactive lines. Claims 16 and 17 describe the dummy metal that aids the heat dissipation with the inactive conductor. Nothing like this is even remotely suggested in the references. Claim 18 calls for the heat sink coupled to the substrate.

Newly added claim 21 calls for "providing a continuous electrically inactive conductor in a dielectric body with dielectric material separating the inactive conductor from a heat dissipating surface that is one of either a bottom silicon substrate connected by bonding to a package or a top surface of an integrated circuit chip connected by bonding to a package, and connecting said electrically inactive conductor to said electrically active interconnect line to dissipate heat therefrom." The electrically inactive conductor is in a dielectric body with dielectric material separating the inactive conductor from a heat dissipating surface and that heat dissipating surface is either a bottom silicon substrate connected by bonding to a package or a top surface of an integrated circuit package. For the reasons discussed above this is not taught in Kazami or Jensen reference.

Claims 22-24 dependent on claim 21 are deemed allowable for at least the same reasons as claim 21. Claim 22 further calls for the electrically inactive conductor to be on one or more metal layers embedded within said dielectric body. Claim 23 dependent on claim 22 further calls for some portions of the electrically inactive conductor are closer to the heat dissipating surface than the electrically active interconnect line, thereby improving its heat dissipating characteristics to said heat dissipating surface. Claim 24 dependent on claim 22 further calls for some portions of said electrically inactive

conductor have larger spatial dimensions in a metallization layer than said electrically active line thereby improving its heat dissipating characteristics to a heat dissipating surface.

In view of the above applicant's claims 1-7, 9-18 and 21 -25 are deemed allowable and an early notice of allowance of these claims is respectfully requested.

Respectfully requested;

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